# RAD1A11ON BEHAVIOR OF ANALOG NEURAL NETWORK CHIP

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## Abstract

Neural networks, based on highly parallel biological systems, Wrfor-in efficient pattern recognit ion and optimizat ion functions because of their capability to "learn" from examples, Since they degrade gracefully with individual device failure, they are suitable for a variety of space, military, and civil applications, providing enhanced speed, autonomy, and intelligence. Both NASA and DOD require VLSI hardware to be space-worthy and hence the degradation behavior of the neural network is of importance. The paper summarisses the neural network experiment conducted for the Space Technology Research Vehicle (STRV) 1-b launched in June 1994.

A set of identical analog feed-forwrd neural network chips was used to study and compare the effects of space and ground radiation on the device characteristics. Reconfigurable synapses as multiplying digital-analog converters with weights stored in digital memory and neurons as variable gain amplifiers with sigmoidal output were used in the feedforward architecture. The network and device characterisitics were monitored in ground-based testing with high energy electron, proton, and gamma radiation; and during geotransfer orbits in flight using shielded and exposed identical VLSI chips.

Ground based degradat ion depended on whether the chips were electrical ly biased during test or not. Unbiased chips were operational to about 100 krads of total dose. Space based radiation was mostly with the chips unbiased, with a total dose of about 11 krads during 228 geotransfer orbits. The slope of the linear part of the synapse-neuron sigmoidal t ransfer curve was found to become steeper with increasing dose. A correlation of the slope degradation was obtained between ground and space radiaiton. This paper provides a summary of the experiments and accumulated and analyzed data, and points out three failure mechani sins.

## introduction

The Space Technology Research Vehicle (STRV) is a development of the United K ingdom's Defense Research Agency (DRA). Two satellites, designated STRV 1-a and 1-b. were launched into a geosynchronous transfer orbit (each orbit of about 10.25 hrs duration) by an Ariane 4 rocket on June 17, 1994. Part of the payload capacity on STRV-1b was taken by the innovative Science and Technology Office of the Ballistic Missile Defense Organization (BMDO/IST) with Jet Propulsion Laboratory (JPL) advanced technology experiments coupled with ground-based testing. Onc of them was the VLSI chip with analog neural network. the results of which are summarized here.

## Neural Net work Architect re

A feedforward neural network architecture was designed for our ground and flight radiation experiments. The chips were fabricated by VLSI Technology Inc. (VTI) using a 2-micron N-well CMOS process through Metal-Oxide-Semiconductor Implementation Service (MOSIS). The chips required a single power supply of -8 volts. consuming less than 80 mW. The chips contained 32 neuron cells and 532 synapse' cells arranged in a partially populated 32 row by 32 column army. A photograph of the chip is shown in Figure 1. The neurons were laid along a diagonal in the array and starting from the left bottom corner, the synapses were placed to the right of the neurons. However, for columns beyond #22, t he synapses were placed in every row position except along the diagonal. "1'bus, the top portion of the circuit on the chip formed a feedback net (however, because of the restricted power and memory budget, no feedback architecture was used in our experiments.

A functional layout of the lower part of the chip is shown in Figure 2. Neuron O (bottom left) is provided an electrical current only externally. Neuron 1 is provided current externally or from neuron O through a synapse at row O, column 1. Neurons 2 through 22 receive current inputs only from onc or many of the previous neurons through the synapses in their respective columns. The last 9 neurons in columns 23 through 31 have 31 synapses connected to the input of each neuron.

## Neuron and Synapse

JPL's analog neural network device designs have been reported in literature [1 ,2]. A neuron is a nonlinear transimpedance amplifier with a sigmoidal transfer function. It has a typical current summing circuit as its input, where the input controls a differential amplifier which controls a current feedback circuit. The neuron's output voltage stage outputs a voltage which is a sigmoidal function of the input current. The gain control circuit is controlled by an externally biased current mirror which is common to all the gain control circuits in all of the

neurons. A high current (-10(.) μA) input to this current mirror will cause the transimpedance function of the neuron to have a more gradual slope in the operating range (+/- 100 μA)[1]. A voltage to current converter is provided for each row to convert the neuron output voltage to an equivalent current input for the synapses in that row. Thus, a multiple current mirror circuit provides identical current signals as input to all the synapses in that row.

A synapse circuit consists of a 7-bit multiplying digital to analog converter (MDAC) and a 7-bit digital memory. This circuit outputs a binary weighted multiple of its analog input current. The input current coming from the neuron in that row is multiplied by the stored digital output weight (integer weight factor between -63 and + 63). Multiplication is accomplished by conditionally scaling the input current by a series of current mirror transistors[2].

Operation of Neural Networks

The synapses in row O or row 1, Fig. 2, were used to provide analog input values to the neural network. Neurons O and 1 could be biased by an external current input so that the synapses in their respective rows would output current when t hcy were programmed with a non-zero weight. In this way, the programmed synapses would force the neurons in their columns to a certain voltage related to the synapse w eights, thus setting the input layer of neurons to the desired input value, The input layer of neurons were connected to a hidden layer of neurons through synapses in the same rows as the input neurons, and in the same columns as the hidden neurons. Likewise, the hidden neurons fed through synapses to a layer of output neurons, Finally the signals from the output neurons were read out one at a time through an analog multiplexer which fed into the analog output buffer.

The chips on ground were exposed to three types of ionizing radiation (electron, proton & gamma rays). Several tests were performed to study the effects of the ionizing radiation on hardware co mponents. The individual radiation experiment was concluded when the neural network chip fa iled and was untestable. Chips under test were either electrically biased or unbiased, The unbiased chips were left with all the pins connected to a conductive foam pad to prevent any charge build-up on the transistors duc to radiation. Biased chips, on the other hand, were powered with an 8 volt supply. Power was supplied to Vdd and ground, and the inputs to the bias transistors were turned "off", i.c. tied either to ground for n-FETs or to Vdd for p-FETs. All of the output pins were left floating and all of the digital inputs were grounded.

The net result was that many of the individual transistors in the chip had no bias applied to their gates, but a large majority of transistors' states were randomly determined each time the chip was powered up, since the synapse memory latches were all uninitialized. Thus, the synapses were in random slate. as were the neurons. The goal of this specific biasing scheme was to avoid CMOS latch-up. Latch-up still occured on a co uple of occasions during radiation exposure.

Chip Tests

For ground testing the neural network chips, mounted On a board with resistors to bias selected chip inputs, power supply connect ions. connectors fort he computer interface. and digital level shifters, were interfaced to a 486/33 PC clone with digital and analog boards plugged into the PC'S ISA bus The interface boards supplied all the necessary digital 1/0's, two 12-bit D/A channels, and one 12-bit A/D channel. Characterization tests were performed for output buffer (linearity check). neuron (sigmoidal curve check), digi tal memory, and synapse-neuron circuits of the neural network chips,

The memory is organized as 532 randomly accessible 7-bit words with 10-bit addresses. q'here are 492 (1024-532) unused memory addresses. The memory test compr ises two tests, a simple memory test and a "walking-ones" memory test, The simple memory test wrote and read all 128 values from -63 to -O and +O to +63 for each of the 532 memory words, In the "walking-ones" memory test, a background pattern was written to all of the addresses. and a foreground pattern (a complement of the background pattern) was written to one address. Then. all the addresses were read back to see if the patterns were written to the appropriate addresses. This was repeated with all of the memory addresses being chosen one at a time to receive the foreground pattern (o test exhaustively for errors in the memory addressing circuits

The synapse-neuron test procedure tests all 532 synapses and 31 of the 32 neurons. Each synapse's output current is swept by programming the M DACs from -63 to +63 and observing the voltage output from t he corresponding neuron. While one of the synapses is being tested, all the other synapses arc programmed to zero to eliminate their effect,

The synapses arc controlled through other neurons at t he input and convoluted through other circuits at the output and arc therefore the hardest components to test These curves show the radiation effects not only on the synapses but on the neurons. the gain-cont rol circuits, and the output buffer. To quantify our observations, a "monotonicity" test was devised. This test compares each point On a synapse's curve with the next more positive point to scc if it was monotonically increasing. The number of non-monotonicities were counted and the degree of error was measured,

## Chip Failure Criteria

Since the chips could fail in a number of different ways, we devised a functionality and failure criteria for the chip as a whole, 1'bus, a chip was considered *non-functional* if any of the following occured: (1) It consumed over 200 mA with an 8 volt power supply (1.6 Watts); (2) The analog performance was so distorted as to make it unusable as a neural network; (3) 80% of the total memory had failed,

## Space Environment Experiments

Two chips with closest match to each other were selected for flight experiments. These chips were mounted and wired on a circuit board, One chip was relatively shielded and the other exposed to the space radiation[3]. Power supply and control logic was assembled on a separate board and the two boards were controlled by an on-board computer, Computer code was developed to characterize the chips in space. Three tests, memory, synapse-neuron, and neural net work learning tests, were performed lasting a few minutes to an hour (during an orbit of- 10 hrs).

## Results (Ground Radiation)

The most significant observation from all of the ground radiation tests was that the biased chips degraded more than an order of magnitude faster than the unbiased ones. The cumulative doses for the unbiased chips were 140 krads for the electron radiation, 250 krads for the gamma radiation, and 440 krads for the proton radiation, The biased chips had much lower cumulative doses of 6 krads for the electron radiation, 7.5 krads for the low dose rate (O. 1 rad /see) gamma radiation, 5 krads for the high dose rate (50 rad/sec) gamma radiation, and 30 krads for proton radiation, Figures 3 and 4 provide an overview of the radiation effects. Figure 3 is a bar char-l showing the chip failures for tbc three ionizing species at different total dose levels for biased and unbiased chips, As can bc seen, the biased chips fail at about 5-7.5 krads of total dose whereas, unbiased chips can tolerate total doses to 200-400 krads before they become nonfunctional. Figure 4 shows the monotonicity errors for the biased and memory errors for the unbiased chips[4].

The results of the ground radiation data with total accumulated dose up to 30 krads were further analyzed The following data (Table I and Fig, 5) depicts the increasing steepness in the slope of the synapse neuron curve based on three synaptic weight values (-1. O, +1, selected in the linear region) for a randomly selected neuron #27 (out of a total of 32) for electron radiation. The data for other neurons are also similar.

Table 1, Neuron output voltage (millivolts) as a function of synaptic weight resolutions for increasing total doses (high energy electrons).

| Synapse Weight | Total Dose (krads) 0 | 5 | 10 | 20 | 30 |
|---|---|---|---|---|---|
| -1.0 | 5303 | 5298 | 5227 | 5098 | 5010 |
| 0.0 | 5398 | 5440 | 5407 | 5355 | 5322 |
| 1.0 | 5498 | 5571 | 5583 | 5586 | 5610 |
| synapse-neuron curve slope (mV/ SW) | 98 | 137 | 181 | 244 | 300 |

It shows that an average change in synapse-neuron curve slope is 6.73 millivolts per synaptic weight per krad. This value is dependent on the electrical gain biases used for the neuron and synapse circuits, and would change the slope considerably when they are changed, This analysis offers a good comparison with the available flight data.

The output buffer test at 30 krads showed initial signs of a distortion ("kink") at the high end, This kink could be seen in all the tests including the neuron tests and the synapse-neuron test, since the output voltage was always measured via the output buffer. The neurons O and 1, and all the synapse-neuron curves continued to show steeper (higher gain) sigmoidal curves with monotonicity errors at 40 krads and beyond.

## Space Environment Effects

TEMPERATURE 't'ES"I'S: The chips mounted on the flight board were tested on ground at different temperatures before launch as the temperature of the circuit board in space was expected to fluctuate between -20 and + 50° C. As the circuit board temperature was monitored during flight, this test permitted the space data to be converted to a common temperature base for proper interpretation. With the characterization at five different

temperatures (-20, 0, 25, 37, and 50 'C) and for seven different weight values (-63, -32, -1, 0, + 1, + 32, and +63) a total of 2240 data points were taken for 32 neurons each on the two flight chips,

The neuron output as a function of synapse weights was plotted as a function of temperature. It was observed that the change in the neuron output was gradual with change in the temperature and could be represented as linear curves for each of the three synaptic weight values (-1, O, and + 1). Using the temperature sensitivity and choosing neuron #27, the flight data were converted to a common temperature of 25° C for three selected synaptic weight values of -1, 0, and +1. Again t hc range of values from -1 to + 1 is in the linear region of the characteristics, and is prone to slope change with radiation dose, This information is used to determine the space radiation effects for the exposed chip,

SPACE DATA: Of the total 31 orbits (from amongst #5 through #2 28) during which neural network experiments were run and data was collected, three orbits, #66, #161, and #228 were selected as representative for data analysis. Even though the first neural network data was taken at Orbit #5, orbit #66 represents the first orbit for which temperature and radiation flux data was available[5]. Orbit #161 is roughly a mid point for which temperature and radiation flux data were available. The exposed and the shielded chips were assumed to be at the same temperature. Figures 6 (a) and (b) show the orbit data for the exposed and shielded chips respectively, giving the neuron output voltages for the three synaptic weights for the three chosen orbits.

Based on the radiation flux data and the times of operation of the chip, it was calculated approximately that the exposed chip received a total dose of approximately 11 krads of radiation when it was unbiased, and only about 120 to 200 rads while biased, Therefore, it is obvious that the radiation effects are primarily due to the 11krads of dose while the chips were unbiased,

Based on this data, calculated slopes of the curves are given in Table 2 as a comparison between shielded and exposed chips. As expected. the shielded chip shows a very small, though measureable, slope change whereas the exposed chip has undergone a significantly larger change in its slope. This behavior is corroborated by that observed in our earlier ground tests (Table 1).

~'able 2. Slope of the synapse-neuron curves given as neuron output in millivolts per unit synaptic weight (mV/sw).

| Chip | Orbit | Total Dose (kRads) | slope (mV/sw) |
|---|---|---|---|
| Shielded | 66 | 0.2 | 167 |
| | 161 | 0.5 | 167 |
| | 228 | 1.0 | 181 |
| Exposed | 66 | 3.0 | 223 |
| | 161 | 6.0 | 2.65 |
| | 288 | 11.0 | 321 |

The synapse neuron curve slope for the chips was about 167 mV/sw with very little radiation, which increased gradually to 321 mV/sw after 11 krads of total dose. Thus a change of slope of 14 mV/sw per krads of total dose was obtained. However, this change in slope did not affect the learning test at all. Similarly, the total dose was not enough to cause any memory damage either.

## Summary

Neural Network analog chips were subjected to degradation on ground using electron, proton, and gamma radiations. Similar chips were flown in geosynchronous transfer orbit and space degradation was analyzed. The data show the following:

a). The unbiased chips continue to perform even with considerable radiation damage.

b). Chips when unbiased continue to function with greater than an order of magnitude higher total dose compared to biased chips.

c). The data shows three failure modes: (l) Steeper synapse-ncu ron curve slope with dose; (2) A left shift of the synapse-neuron curve duc to increased synapse. current leakage; and (3) Failure of digital memories.

These experiments have demonstrated graceful degradation and fault tolerant performance of neural networks in harsh space environment and a potential for usc of neural network architectures for future space missions.

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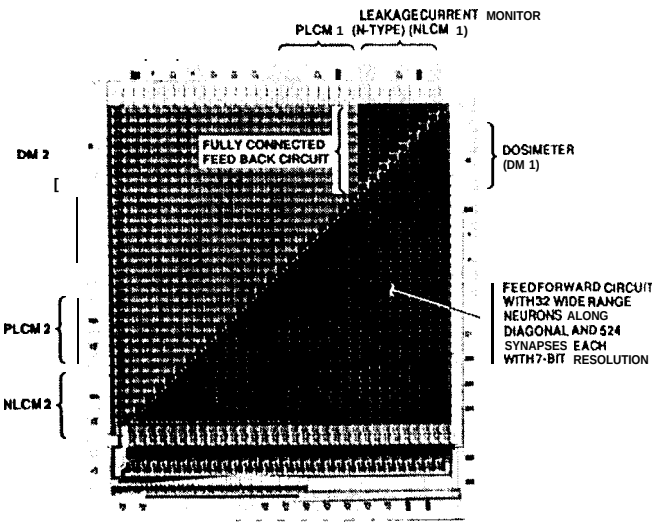


Figure 1, A photograph of the STRV/NN chip, showing the 32x32 partially filled synapse-neuron array. '1'here are 32 neurons along the diagonal and 532 synapses in the array.

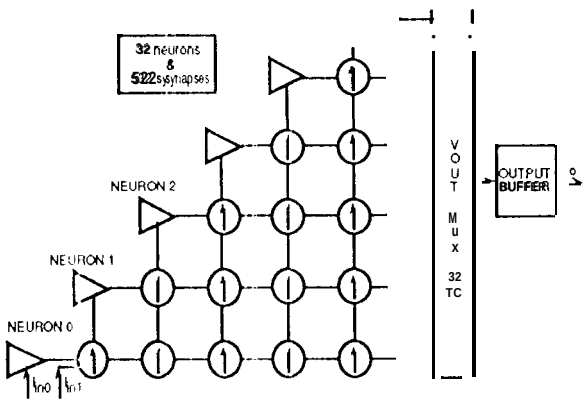


Figure 2. Functional layout of a part of the neural network chip, Triangles along the diagonal arc neurons and sy names are in the array as circles, The 32-neuron outputs are multiplexed and obtained individually via a unity gain output buffer.

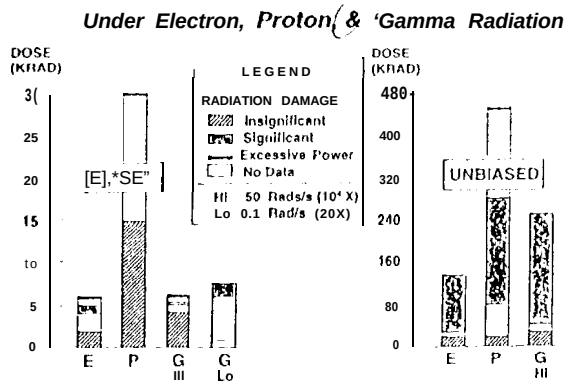


Figure 3. A bar chart showing the overall degradation with the three species of radiation source for biased and unbiased neural network chips. For biased chips, two dose rates, 0.1 and 50 rad/s. were used with gamma radiation.

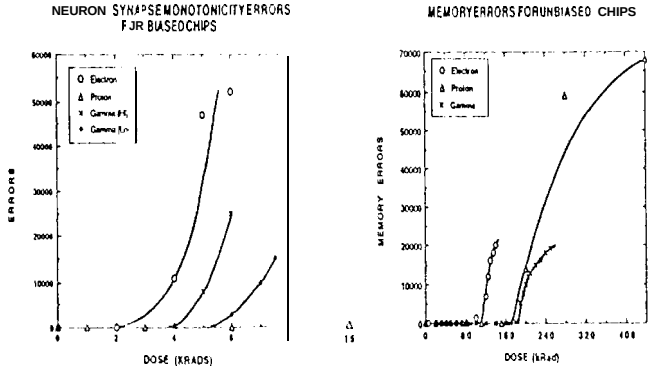


Figure 4. Results of the monotonicity errors vs. total dose for the biased chips and memory errors with total dose for the unbiased chips, Biased chip did not show any memory degradation with proton damage up to 1S krads but became non functional at the next level of measurement at 30 krads.

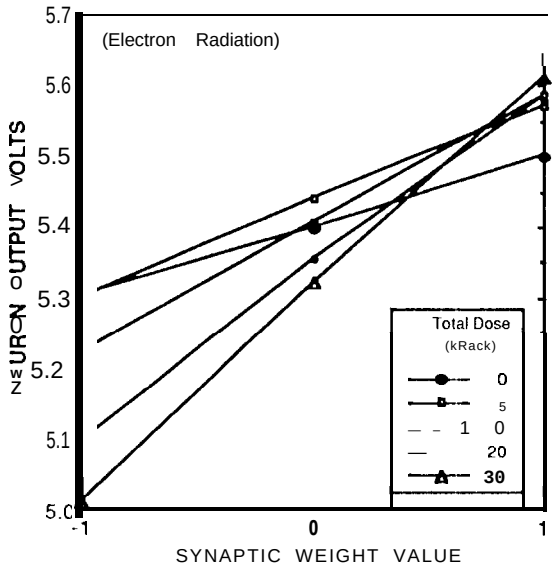


Figure S, Variation of the slope of the linear region of the synapse-mlron curve for neuron #27, for high energy electron radiation from 0 to 30 krads total dose,

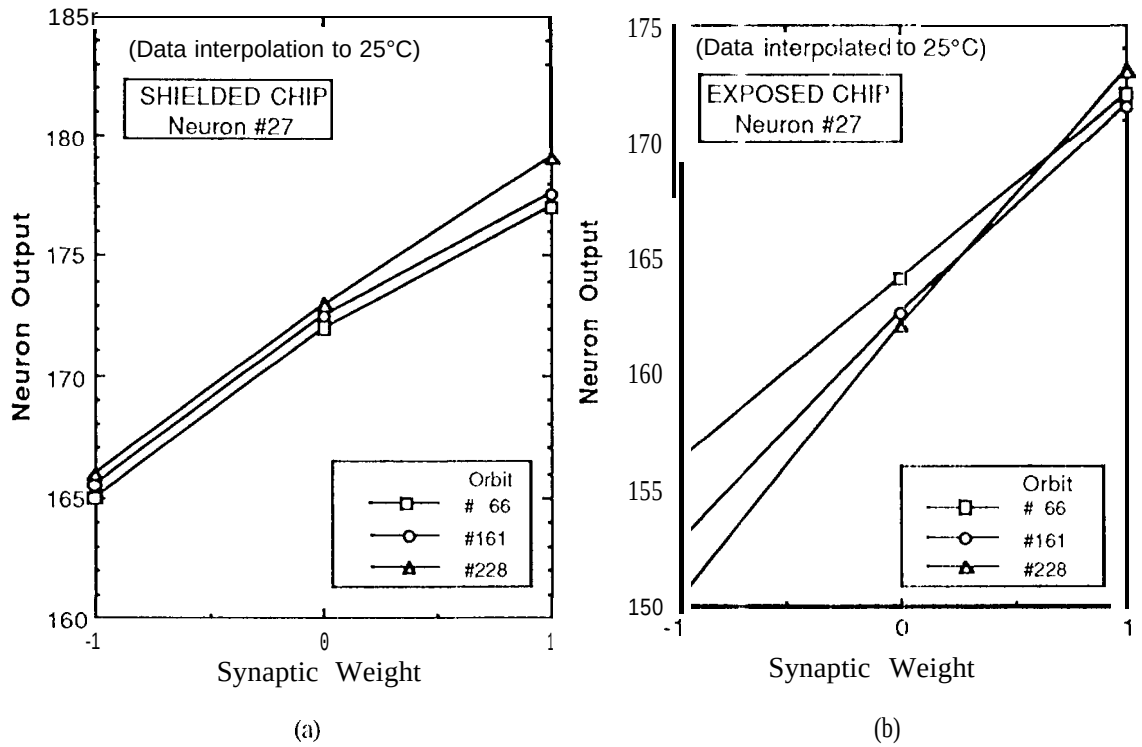


Figure 6. The neuron #27output(Outputin millivolts =- DAC valuu/255*71 10) vs synaptic weight for three total doses in space for (a) shielded; and (b) exposed chips.